SRI SHAKTHI

INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution, Affiliated to Anna University)
Coimbatore – 62.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CURRICULA AND SYLLABI

M.E – VLSI DESIGN REGULATION – 2021

SRI SHAKTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY, COIMBATORE
(AUTONOMOUS)
M E VLSI DESIGN
REGULATIONS – 2021

PROGRAMME EDUCATIONAL OBJECTIVES:

PEO1	:	To equip the graduates with in-depth knowledge on new technical ideas, to analyse and evaluate the potential engineering problems and contribute to research and development in core areas using modern engineering and IT Tools.
PEO2	:	To demonstrate self -management and teamwork in collaborative and multidisciplinary area
PEO3	:	To inculcate good professional practices with responsibility to contribute to sustainable development of society
PEO4		To have a zeal for improving technical competency by continuous and corrective learning

PROGRAMME OUTCOMES:

Engineering Graduates will be able to:

PO1	a	Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	b	Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	c	Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	d	Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	e	Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	f	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	g	Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	h	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	i	Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	j	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	k	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work,

as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 l Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OBJECTIVES (PSOs)

PSO1 : Design and develop VLSI circuits to optimise power and area requirements, free from faults and dependencies by modelling, simulation and testing

PSO2 : Develop VLSI systems by learning advanced algorithms, architecture and software – hardware design

PSO3 : Communicate engineering concepts effectively by exhibiting high standards of technical presentation and scientific documentations.

MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMME OUTCOMES

A broad relation between the programme objective and the outcomes is given in the following table

PROGRAMME EDUCATIONAL OBJECTIVES	PROGRAMME OUTCOMES											
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**	**L**
1	1	1	1	1	1	3	3	3	2	3	3	2
2	1	2	2	2	3	1	1	1	1	2	1	2
3	2	2	2	2	2	3	3	3	3	1	3	1

1. Strong 2. Significant 3. Reasonable

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M E VLSI DESIGN
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CHOICE BASED CREDIT SYSTEM

MAPPING OF COURSE OUTCOMES WITH PROGRAMME OUTCOMES:

A broad relation between the Course Outcomes and Programme Outcomes is given in the following table

COURSE OUTCOMES		PROGRAMME OUTCOMES											
Sem	Course Name	A	B	C	D	E	F	G	H	I	J	K	L
I	Applied Mathematics for Electronics Engineers	✓	✓	✓	✓							✓	✓
	Advanced Digital system design	✓	✓	✓		✓	✓			✓		✓	✓
	CMOS digital VLSI design	✓	✓	✓	✓	✓	✓					✓	✓
	DSP Integrated circuits	✓	✓	✓	✓	✓	✓					✓	✓
	CAD for VLSI circuits	✓	✓	✓	✓	✓	✓					✓	✓
	Design Verification	✓	✓	✓	✓	✓	✓					✓	✓
	Advanced Digital system design Laboratory	✓	✓	✓	✓	✓	✓					✓	✓
	CMOS digital VLSI design Laboratory	✓	✓	✓	✓	✓	✓					✓	✓
	DSP Integrated circuits Laboratory	✓	✓	✓	✓	✓	✓					✓	✓
	CAD for VLSI circuits Laboratory	✓	✓	✓	✓	✓	✓					✓	✓
	Design Verification Laboratory	✓	✓	✓	✓	✓	✓					✓	✓
	VLSI design project I	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓
	Audit Course												
II	Testing of VLSI Circuits	✓	✓	✓	✓	✓	✓					✓	✓
	VLSI Signal Processing	✓	✓	✓	✓	✓	✓					✓	✓
	Research Methodologies	✓	✓	✓	✓							✓	✓
	Professional Elective I												
	Professional Elective II												
	Professional Elective III												
	Testing of VLSI Circuits Laboratory	✓	✓	✓	✓	✓	✓					✓	✓
	VLSI Signal Processing Laboratory	✓	✓	✓	✓	✓	✓					✓	✓
	VLSI Design Project II	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓
	Technical Seminar	✓			✓					✓	✓	✓	✓
	Audit Course												
III	Professional Elective IV												
	Professional Elective V												
	Project Work Phase I	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓
IV	Project Work Phase II	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓

SRI SHAKTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY, COIMBATORE
(AUTONOMOUS)
M E VLSI DESIGN
REGULATIONS – 2021
CHOICE BASED CREDIT SYSTEM
I - IV SEMESTERS CURRICULA AND SYLLABI

SEMESTER I

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1	21MS105	Applied Mathematics for Electronics Engineers	BS	4	3	1	0	4
2	21VD101	Advanced Digital system design	PC	3	3	0	0	3
3	21VD102	CMOS digital VLSI design	PC	3	3	0	0	3
4	21VD103	DSP Integrated circuits	PC	3	3	0	0	3
5	21VD104	CAD for VLSI circuits	PC	3	3	0	0	3
6	21VD105	Design Verification	PC	3	3	0	0	3
7	21AC101	Audit Course - 1	HS	2	2	0	0	0
PRACTICALS								
8	21VD112	Advanced Digital system design Laboratory	PC	2	0	0	2	1
9	21VD113	CMOS digital VLSI design Laboratory	PC	2	0	0	2	1
10	21VD114	DSP Integrated circuits Laboratory	PC	2	0	0	2	1
11	21VD115	CAD for VLSI circuits Laboratory	PC	2	0	0	2	1
12	21VD116	Design Verification Laboratory	PC	2	0	0	2	1
13	21VD111	VLSI design project I	EEC	6	0	0	6	3
		TOTAL		**37**	**20**	**1**	**16**	**27**

SEMESTER II

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1	21VD201	Testing of VLSI Circuits	PC	3	3	0	0	3

2	21VD202	VLSI Signal Processing	PC	3	3	0	0	3
3	21CC201	Research Methodologies	PC	3	3	0	0	3
4	21PVD16	Professional Elective I	PE	2	2	0	0	2
5	21PVD23	Professional Elective II	PE	2	2	0	0	2
6	21PVD10	Professional Elective III	PE	2	2	0	0	2
7	21AC201	Audit Course 2	HS	2	2	0	0	0
PRACTICALS								
8	21VD212	Testing of VLSI Circuits Laboratory	PC	2	0	0	2	1
9	21VD211	VLSI Design Project II	EEC	6	0	0	6	3
10	21VD213	Technical Seminar	EEC	2	0	0	2	1
		TOTAL		**32**	**20**	**0**	**12**	**24**

SEMESTER III

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1	21PVD21	Professional Elective IV	PE	3	3	0	0	3
2	21PVD22	Professional Elective V	PE	3	3	0	0	3
PRACTICALS								
3	21VD311	Dissertation Phase I/ Industrial Project	EEC	12	0	0	12	6
		TOTAL		**18**	**6**	**0**	**12**	**12**

SEMESTER IV

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1	21VD411	Project Work Phase II	EEC	**24**	**0**	**0**	**24**	**12**
				TOTAL NO. OF CREDITS:75				

LIST OF ELECTIVES

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
ELECTIVE 1								
1	21PVD01	Device Modeling - I	PE	4	2	0	2	3
2	21PVD02	RF IC Design	PE	4	2	0	2	3
3	21PVD13	Selected Topics in ASIC Design	PE	4	2	0	2	3
4	21PVD11	Reconfigurable Architectures	PE	4	2	0	2	3
5	21PVD14	Design and Analysis of Computer Algorithms	PE	4	2	0	2	3
6	21PVD18	Scripting Languages for VLSI	PE	4	2	0	2	3
ELECTIVE 2								
1	21PVD03	Design of Analog Filters and Signal Conditioning Circuits	PE	4	2	0	2	3
2	21PVD04	Nano Scale Devices	PE	4	2	0	2	3
3	21PVD12	Advanced Microprocessors and Architectures	PE	4	2	0	2	3
4	21PVD15	Device Modeling- II	PE	3	3	0	0	3
5	21PVD22	Smart Antennas	PE	3	3	0	0	3
ELECTIVE 3								
1	21PVD05	DSP Architectures and Programming	PE	4	2	0	2	3
2	21PVD06	Networks on Chip	PE	4	2	0	2	3
3	21PVD17	MEMS and NEMS	PE	4	2	0	2	3
4	21PVD23	Antenna Technologies and Design	PE	3	3	0	0	3
5	21PVD19	Hardware – Software Co- Design	PE	4	2	0	2	3
ELECTIVE 4								
1	21PVD07	Signal Integrity for High Speed Design	PE	4	2	0	2	3
2	21PVD08	Digital Control Engineering	PE	4	2	0	2	3
3	21PVD16	Digital Image Processing	PE	3	3	0	0	3
4	21PVD20	Selected Topics in IC Design	PE	4	2	0	2	3

ELECTIVE 5								
1	21PVD09	Embedded System Design	PE	4	2	0	2	3
2	21PVD10	Soft Computing and Optimization Techniques	PE	4	2	0	2	3
3	21PVD21	Low Power VLSI Design	PE	3	3	0	0	3

Audit Courses								
SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1	21AC101	English for Research Paper Writing	HS	2	2	0	0	0
2	21AC201	Disaster Management	HS	2	2	0	0	0
3	21AC301	Stress Management by Yoga	HS	2	2	0	0	0
4	21AC401	Value Education	HS	2	2	0	0	0

SUMMARY

S.No	**SUBJECT AREA**	**CREDITS AS PER SEMESTER**				**CREDITS TOTAL**
		I	**II**	**III**	**IV**	
1.	**HS**					
2.	**BS**	4				4
3.	**ES**					
4.	**PC**	20	11			31
5.	**PE**		9	6		15
6.	**EEC**	3	4	6	12	25
Total		27	24	12	12	75

21MS105	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	L	T	P	C
		3	1	0	4

COURSE OBJECTIVES

The main objective of this course is to demonstrate various analytical skills in applied mathematics and extensive experience with the tactics of problem solving and logical thinking applicable in electronics engineering. This course also will help the students to identify, formulate, abstract, and solve problems in electrical engineering using mathematical tools from a variety of mathematical areas, including fuzzy logic, matrix theory, Fourier series, dynamic programming and queuing theory.

PRE-REQUISITES:

- Basic concepts of Logic
- Basic concepts of Matrices
- Basic concepts of Differentiation
- Basic concepts of Integration

UNIT I FUZZY LOGIC **12**

Classical logic –Multivalued logics –Fuzzy propositions –Fuzzy quantifiers.

UNIT II MATRIX THEORY **12**

The Cholesky decomposition – Generalized Eigenvectors – QR factorization – Least squares method – Singular value decomposition

UNIT III FOURIER SERIES **12**

Fourier trigonometric series (concepts only): Periodic function as power signals – Convergence of series – Even and odd function: Cosine and sine series – Non periodic function : Extension to other intervals – Power signals : Exponential Fourier series – Parseval's theorem and power spectrum – Eigenvalue problems and orthogonal functions.

UNIT IV DYNAMIC PROGRAMMING **12**

Dynamic programming –Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality

UNIT V QUEUEING MODELS **12**

Poisson Process – Markovian queues – Little's formula – Single and Multi - Server models – Steady state analysis – Self-service queue.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Apply the concepts of fuzzy sets, Fuzzy logic, prepositions and fuzzy quantifiers for solving the real time problems.

CO2 Apply various methods in matrix theory to solve system of linear equations.

CO3 Solve the problem using the Fourier series analysis.

CO4 Apply the dynamic programming techniques in the Engineering problems

CO5 Expose the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.

CO6 Apply and expose the techniques for an application.

REFERENCE BOOKS

1. Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.
2. George, J. Klir. and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and Applications", Prentice Hall of India Pvt. Ltd., 1997.
3. Gross, D., Shortle J. F., Thompson, J.M., and Harris, C. M.,"Fundamentals of Queueing Theory", 4th Edition, John Wiley, 2014.
4. Johnson, R.A., Miller, I and Freund J., "Miller and Freund's Probability and Statistics for Engineers", Pearson Education, Asia, 8thEdition, 2015.
5. Taha,H.A.,"Operations Research:An Introduction", 9th Edition, Pearson Education, Asia, New Delhi, 2016.

Total:60 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	2		1				1	1	1	2	3	
CO2	3		2	2		1				1	1	1	2	3	
CO3	3		2	2		1				1	1	1	2	3	
CO4	3	2	2	2		1				1	1	1	2	3	
CO5	3	2	2	2		1				1	1	1	2	3	
CO6	3	2	2	2		1				1	1	1	2	3	

21VD101	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

- To introduce methods to analyze and design synchronous and asynchronous Sequential circuits
- To introduce the architectures of programmable devices
- To introduce design and implementation of digital circuits using programming tools

UNIT I SEQUENTIALCIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuitsASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIALCIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in selftest

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

COURSE OUTCOMES

At the end of the course, a student will be able to

CO1 Analyse and design sequential digital circuits

CO2 Identify the requirements and specifications of the system required for a given application

CO3 Design and use programming tools for implementing digital circuits of industry Standards.

CO4 Design and analyse of a synchronous devive ,

CO5 Study of system design and implementation.

CO6 Design and implementation of Digital circuits,

REFERENCE BOOKS

1. CharlesH.Roth Jr "Fundamentals of Logic Design" Thomson Learning2004.

2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL,Prentice Hall,1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR),1999.
4. Nripendra N Biswas "Logic Design Theory" Prentice Hall ofIndia,2001.
5. ParagK.Lala "Fault Tolerant and Fault Testable Hardware Design" BS Publications,2002
6. ParagK.Lala "Digital system Design using PLD" B SPublications,2003
7. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson ,2003.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	1	3	2						1	2	1	3	2	
CO2	3	1		2						1	2	1	3	2	
CO3	3	1	3	2						1		1	3	2	
CO4	3	1	3							1	2	1	3	2	
CO5	3	1	3							1	2	1	3	2	
CO6	3	1	3	2						1	2	1	3	2	

21VD112	ADVANCED DIGITAL SYSTEM DESIGN LABORATORY	L	T	P	C
		0	0	2	1

List of Experiments:

1. Design of Inverter and all logic gates
2. Design and Simulation of Full adder
3. Design and Simulation of Serial Binary Adder, Carry Look Ahead Adder.
4. Design of SRAM and DRAM
5. Design of pseudo logic gates
6. Design of DCVSL logic gates
7. Design of flip flops: SR, D, JK, T
8. Design of edge triggered registers
9. Design of barrel shifter
10. Design of Multiplier

Total:15 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	2	3	1				1	1	1	3	1	
CO2	3	2		2	3	1				1	1	1	3	1	
CO3	3	2	2	2	3	1				1	1	1	3	1	
CO4	3	2	2	2	3	1				1	1	1	3	1	
CO5	3	2	2	2		1				1	1	1	3	1	
CO6	3	2	2	2	3	1				1	1	1	3	1	

21VD102	CMOS DIGITAL VLSI DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

- This course deals comprehensively with all aspects of transistor level design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.
- The focus will be on the transistor level design and will address all important issues related to size, speed and power consumption. The units are classified according to the important building and will introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.

THEORY COMPONENT CONTENTS

UNIT I MOS TRANSISTOR PRINCIPLES ANDCMOS INVERTER 9

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore‟s constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES 9

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.

CO2 Discuss design methodology of arithmetic buildingblock

CO3 Analyze tradeoffs of the various circuit choices for each of the buildingblock.

CO4 Study of memory devices.

CO5 Discuss the concepts of interconnect and clocking mdoels.

CO6 Study and analyze of CMOS circuits.

REFERENCE BOOKS

1. JanRabaey, AnanthaChandrakasan, B Nikolic, “Digital Integrated Circuits: A Design Perspective”. Second Edition, Feb 2003, Prentice Hall of India.

2. Jacob Baker “CMOS: Circuit Design, Layout, and Simulation, Third Edition”, Wiley IEEE Press 2010 3rd Edition.
3. M J Smith, “Application Specific Integrated Circuits”, Addisson Wesley,1997
4. N.Weste, K. Eshraghian, “ Principles of CMOS VLSI Design”. Second Edition, 1993 Addision Wesley.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	2	1					1	1	2	3	2	1
CO2	3	2	2	2	1					1	1	2	3	2	1
CO3	3	2	2		1					1	1	2	3	2	1
CO4	3	2	2	2	1					1	1	2	3	2	1
CO5	3	2	2	2	1					1	1	2	3	2	1
CO6	3	2	2	2	1					1	1		3	2	1

21VD113 CMOS DIGITAL VLSI DESIGN LABORATORY L T P C

0 0 2 1

List of Experiments:

1. Understanding Synthesis principles. Backannotation.
2. Study on FPGA kit and synthesis procedures.
3. Test vector generation and timing analysis of sequential logic design using HDL languages.
4. Combinational logic design realized using HDL languages.
5. FPGA real time programming and I/O interfacing.
6. Understanding Synthesis principles. Backannotation.
7. Test vector generation and timing analysis of sequential using HDLlanguages
8. Combinational logic design realized using HDL languages.

Total:15 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	3	2	1	1				1	2	1	2	2	
CO2	3	2	3	2	1	1				1	2		2	2	
CO3	3	2	3	2	1	1				1	2	1	2	2	
CO4	3	2	3	2	1	1				1	2	1	2	2	
CO5	3	2	3	2	1	1				1		1	2	2	
CO6	3	2	3	2	1	1				1	2	1	2	2	

21VD103	DSP INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multirate systems and finite word length effects
- To know about the basic DSP processor architectures and the synthesis of the processing elements

UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS 9

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise

UNIT III DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and mpulti computers, Systolic and Wave front arrays, Shared memory architectures.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES 9

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks-Storage elements – clocking of synchronous systems, Asynchronous systems-FSM

UNIT V ARITHMETIC UNIT AND PROCESSING ELEMENTS 9

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor

COURSE OUTCOMES

At the end of the course, a student will be able to

CO1 Get to know about the Digital Signal Processing concepts and its algorithms

CO2 Get an idea about finite word length effects in digital filters

CO3 Concept behind multi rate systems is understood.

CO4 Get familiar with the DSP processor architectures and how to perform synthesis of processing elements.

CO5 Study of arthimetic and processing elements.

CO6 Study and analyze of DSP Integrated circuits.

REFERENCE BOOKS

1. B.Venkatramani, M.Bhaskar, “Digital Signal Processors”, Tata McGraw-Hill,2002.
2. John J. Proakis, Dimitris G. Manolakis, “Digital Signal Processing”, Pearson Education,2002.
3. KeshabParhi, “VLSI Digital Signal Processing Systems design & Implementation”, John Wiley & Sons,1999.
4. Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York,1999.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	2	1						1	1	3	1	
CO2	3	2		2	1						1	1	3	1	
CO3	3	2	2	2	1						1	1	3	1	
CO4	3	2	2	2	1						1	1	3	1	
CO5		2	2	2	1						1	1	3	1	
CO6	3	2	2	2	1						1	1	3	1	

21VD114 DSP INTEGRATED CIRCUITS LABORATORY

L	T	P	C
0	0	2	1

List of Experiments

1. To verify linear convolution and correlation.
2. To find and sketch impulse and step response.
3. To find the FFT of given 1-D signal and plot.
4. To verify circular convolution.
5. FIR filter design using different window techniques.
6. IIR filter design using analog approximations.
7. Spectrum Analysis using DFT.
8. To study the architecture of DSP chips TMS 320C6X and instruction set.

Total:15 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	3	2	2					1	1	2	3	2	
CO2	3	2	3	2	2					1		2	3	2	
CO3	3	2	3	2	2					1	1	2	3	2	
CO4	3	2		2	2					1	1	2	3	2	
CO5	3	2	3	2	2					1	1	2	3	2	
CO6	3	2	3	2	2					1	1	2	3	2	

21VD104	CAD FOR VLSI CIRCUITS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

The students should be made to:

- Learn VLSI Design methodologies
- Understand VLSI design automation tools
- Study modeling and simulation

UNIT I INTRODUCTION TO VLSI DESIGN FLOW 9

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II LAYOUT, PLACEMENT AND PARTITIONING 9

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

UNIT III FLOOR PLANNINGAND ROUTING 9

Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV SIMULATION AND LOGIC SYNTHESIS 9

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS 9

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

COURSE OUTCOMES

At the end of the course, a student will be able to

CO1 Outline floor planning and routing

CO2 Explain Simulation and Logic Synthesis

CO3 Discuss the hardware models for high level synthesis.

CO4 Study and implementation of simulation.

CO5 Design of high level synthesis circuits.

CO6 Analyze of VLSI circuits and implementation.

REFERENCE BOOKS

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", KluwerAcademic Publishers,2002.
2. S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002
3. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World Scientific1999

4. StevenM.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing1987.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	2	2	1	1					2	1	1	2	1	
CO2	3	2		1	1					2	1	1	2	1	
CO3	3	2	2	1	1					2	1	1	2	1	
CO4	3	2	2							2	1	1	2	1	
CO5	3	2	2	1	1					2	1	1	2	1	
CO6	3	2	2	1	1					2	1	1	2	1	

21VD115	CAD FOR VLSI CIRCUITS LABORATORY	L	T	P	C
		0	0	2	1

List of Experiments:

1. Verification of design functionality implemented in FPGA by capturing the signal in DSO.
2. Real time application development.
3. Design Entry Using VHDL or Verilog examples for Digital circuit descriptions using HDL languages
4. Testing a sequential program method in HDL for Digital circuit,
5. Concurrent statements program method in HDL for Digital circuit.
6. Structural description program method in HDL for Digital circuit.
7. FPGA real time programming and I/Ointerfacing.
8. Interfacing with Memory modules in FPGA Boards.

Total:15 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	3	2	1						1	2	2	1	2	
CO2	3	3	2	1						1	2	2	1	2	
CO3	3	3	2	1						1	2	2	1	2	
CO4	3			1						1	2	2	1	2	
CO5	3	3	2	1						1	2	2	1	2	
CO6	3	3	2	1						1	2	2	1	2	

21VD105	DESIGN VERIFICATION	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

- To introduce verification of hardware designs.
- To provide a practical approach for verification of designs.
- To give an introduction to FPGA based verification and Emulation of VLSI systems.

UNIT I INTRODUCTION TO VERIFICATION 9

Introduction to Verification– Need for Functional Verification –Validation and Emulation– ASIC Verification Concepts– Bottle Neck Problem in ASIC Design Challenges– Design – FPGA and Emulation based Validation and Testing –Major Verification Tasks – Creating Verification Plan – Linear Test Bench – Linear Random Test Bench– Self Checking Test Benches – Test Coverage. Formal Verification–Decision Diagrams – Equivalence Checking.

UNIT II SYSTEM VERILOG FOR DESIGN 9

System Verilog for Design–Standard Data Types and Literals –Procedures and Procedural Statements – Operators– User-Defined Data Types – Hierarchy and Connectivity –Tasks and Functions – Interfaces

UNIT III SYSTEM VERILOG FOR VERIFICATION 9

System Verilog for Verification–Verification Blocks –Transaction– Level Modeling– System Verilog Classes – Random Stimulus – Class-Based Randomization – Functional – Coverage – Queues and Dynamic Arrays– Interprocess Synchronization – Direct Programming Interface(DPI).

UNIT IV SYSTEM VERILOG ASSERTIONS 9

System Verilog Assertions– Assertion-Based Verification (ABV) – Immediate and Concurrent Assertions – Simple Boolean Assertions – Sequences –Sequence Composition – Advanced SVA Features – Coding Guidelines– Functional Coverage -Practical SVA Application.

UNIT V INTRODUCTION TO OVM/UVM VERIFICATION 9

Introduction to Static Formal Verification–OVM/UVM Verification Components and Objects – OVM/UVM Transactions –OVM/UVM Factory Basics.

COURSE OUTCOMES

At the end of the course, a student will be able to

CO1 Familiarize verification process and its different methodologies

CO2 Write test-benches using system verilog in an efficient way

CO3 Develop algorithms which can automate the design verification process.

CO4 Design of high level synthesis circuits.

CO5 Study of OVM/UVM

CO6 Study and implement in the VLSI application.

REFERENCE BOOKS

1. Chris Spear, System Verilog for Verification: A Guide to Learning the Test Bench Language Features, Third Edition, Springer,2012.
2. Douglas Perry, and Harry Foster, Formal Verification: For Digital Circuit Design, First Edition, McGraw-Hill Education,2005.
3. S Halsoun and T Sasao, Logic Synthesis and verification, Kluwer Academic publishers, 2002
4. PallabDasgupta, A Road Map for Formal Property Verification, Springer 2006.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	1	2	1					1	2	1	2	1	
CO2	3			2	1							1	2	1	
CO3	3	2	1	2	1							1	2	1	
CO4	3	2	1	2	1					1	2	1	2	1	
CO5	3	2	1		1					1	2	1	2	1	
CO6	3	2	1	2	1					1	2	1	2	1	

21VD116	DESIGN VERIFICATION LABORATORY	L	T	P	C
		0	0	2	1

List of Experiments:

1. Design an adder and 4-bit full adder. Instantiate four 4-bit adders to add two16 bit values, implement in FPGA using switches as input and LED as the output. Refer synthesis report regarding the area, power and speed.
2. Using a simulator(SPICE/CADENCE/Synopsis) build a Fulladder schematic using built-in gates.
3. Build standard libraries(Inverter, NAND, NOR and AOI) for a given technology using CADENCE/Synopsis. Do DRC, LVS and Extraction.
4. Develop the behavioural style HDL code for D-Flip Flop using gated, positive edge andnegative edge clock modes.
5. Develop the behavioural style HDL code for 4-bit counter.Develop the structural style HDL code for 4-bit counter using T Flip Flop (use of generate statement, area-performance analysis after synthesize). Compile, synthesize and simulate each design entity and verify the functionality by creatingvector waveform file.
6. Design a traffic light controller for an intersection with a main street, a side street, and a pedestrian crossing or a Vending Machine(Implement it on FPGA)
7. Using the NAND and NOR standard cells designed in Exp 3, draw the layout for D and SR latch. Do DRC, LVS and Extraction.
8. Implement a 4-bit ALU.
9. Verification examples using System Verilog.

Total:15 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	1	2	1					1	2	1	2	1	
CO2	3			2	1					1	1				
CO3	3	3		2	1					1	3		1		
CO4	3		2	2	1					1	2	2		2	
CO5	3		1		1					1	2				
CO6	3	1		2	1					1	2	1	2	1	

21VD201	TESTING OF VLSI CIRCUITS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

The students should be made to:

- Understand logic fault models
- Learn test generation for sequential and combinational logic circuits

PRE-REQUISITES: P19VLTL104

UNIT I TESTING AND FAULT MODELLING 9

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models –Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION 9

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design– system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Selfchecking design – System Level Diagnosis.

COURSE OUTCOMES

At the end of the course, a student will be able to

CO1 Prepare design for testability.

CO2 Discuss test algorithms.

CO3 Explain fault diagnosis.

CO4 Perform VLSI based experiments using / CADENCE/ TANNER/ Mentor/Synopsis.

CO5 Analyze and implementation of fault diagnosis.

CO6 Used to test the VLSI circuits.

REFERENCE BOOKS

1. A.L.Crouch, “Design Test for Digital IC‟s and Embedded Core Systems”, Prentice all International,2002.
2. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House,2002.
3. M.L.Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory andMixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press,2002.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3			1		1						2	3	2	
CO2	3			1		1								2	
CO3	3	3	2	1		1								2	
CO4	3	3	2	1		1						2	3	2	
CO5	3	3	2	1		1						2	3	2	
CO6	3	3	2	1		1						2	3	2	

21VD212	TESTING OF VLSI CIRCUITS LABORATORY	L	T	P	C
		0	0	2	1

List of Experiments:

1. To synthesize and understand the Boolean optimization in synthesis.
2. Static timing analyses procedures and constraints.
3. Critical path considerations.
4. Scan chain insertion, Floor planning, Routing and Placement procedures.
5. Power planning, Layout generation, LVS and back annotation, Total power estimate.
6. Analog circuit simulation.
7. Simulation of logic gates, Current mirrors, Current sources, Differential amplifier in Spice.
8. Layout generations, LVS, Back annotation

Total:15 Periods

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair												CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3			1		1						2	3	2	
CO2	3			1		1								2	
CO3	3	3	2	1		1								2	
CO4	3	3	2	1		1						2	3	2	
CO5	3	3	2	1		1						2	3	2	
CO6	3	3	2	1		1						2	3	2	

21VD202	VLSI SIGNAL PROCESSING	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS **9**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE-I **9**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III ALGORITHIMIC STRENGTH REDUCTION-II **9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES **9**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

UNIT V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING **9**

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Ability to modify the existing or new DSP architectures suitable for VLSI

CO2 Multi resolution techniques using MATLAB software

CO3 Analyze spectral estimation methods along with PCA/ICA analysis.

CO4 Design and analyze of bit-level circuits.

CO5 Design and study of asynchronous pipelining.

CO6 Implementation of DSP architectures in VLSI.

REFERENCE BOOKS

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience,2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition,2004.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	3	2							2	3	2	
CO2	3	2	2									2			
CO3	3	2	2	3	2							2			
CO4	3	2	2	3	2							2	3	2	
CO5	3	2	2									2	3	2	
CO6	3	2	2	3	2							2	3	2	

21VD202	VLSI SIGNAL PROCESSING	L	T	P	C
		0	0	2	1

List of Experiments:

1. Signal Decomposition using Multi Resolution Techniques
2. Wavelet Coding Techniques
3. Spectral Estimation using Parametric Method
4. Higher Order Statistics of a Signal, PCA/ICA Analysis.

Total:15 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	2	1	2	3	2					1	3	1	2	
CO2	3	2	1	2	3	2					1	3	1	2	
CO3	3	2	1	2	3	2					1	3	1	2	
CO4	3	2	1	2	3	2					1	3	1	2	
CO5	3	2	1	2	3	2					1	3	1	2	
CO6	3	2	1	2	3	2					1	3	1	2	

21CC201	RESEARCH METHODOLOGIES	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

- Ability to critically evaluate current research and propose possible alternate methods for further work.
- Ability to develop hypothesis / Problem Statement and methodology for research.
- Ability to comprehend and deal with complex research issues in order to communicate their scientific results clearly for peer review.

UNIT I INTRODUCTION TO RESEARCH METHODOLOGY **9**

Meaning of Research, Types of Research, Research Process, Problem definition, Objectives of Research, Research Questions, Research design, Approaches to Research, Quantitative vs. Qualitative Approach, Understanding Theory, Building and Validating Theoretical Models, Exploratory vs. Confirmatory Research, Experimental vs Theoretical Research, Importance of reasoning in research.

UNIT II LITERATURE REVIEW **9**

Problem Formulation, Understanding Modeling & Simulation, Conducting Literature Review, Referencing, Information Sources, Information Retrieval, Role of libraries in Information,Retrieval, Tools for identifying literatures, Indexing and abstracting services, Citation indexes.

UNIT III DATA COLLECTION AND SAMPLING DESIGN **9**

Experimental Research: Cause effect relationship, Development of Hypothesis, Measurement Systems Analysis, Error Propagation, Validity of experiments, Statistical Design of Experiments, Field Experiments, Data/Variable Types & Classification, Data collection, Numerical and Graphical Data Analysis: Sampling, Observation, Surveys, Inferential Statistics, and Interpretation of Results

UNIT IV RESEARCH REPORTS **9**

Preparation of Dissertation and Research Papers, Tables and illustrations, Guidelines for writing the abstract, introduction, methodology, results and discussion, conclusion sections of a manuscript. References, Citation and listing system of documents

UNIT V INTELLECTUAL PROPERTY RIGHTS (IPR) AND PATENTS **9**

Intellectual property rights (IPR) - patents-copyrights-Trademarks-Industrial design geographical indication. Ethics of Research- Scientific Misconduct- Forms of Scientific Misconduct. Plagiarism, Unscientific practices in thesis work, Ethics in science

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Recognize the importance of literature review.
CO2 Identify the different types of research.
CO3 Formulate problem statement and develop mathematical models for different problems.
CO4 Formulate methodology of research and experimental analysis.
CO5 Analyze the results using statistical methods, interpretation of results with reference to similar research outcomes.
CO6 Prepare technical reports and research papers.

TEXT BOOKS

1. C.R. Kothari, Research Methodology Methods and Techniques, 2ndRevised edition, New Age
2. R. Panneerselvam, "Research Methodology", PHI2004

REFERENCE BOOKS

1. Deepak Chawla, Neena Sodhi "Research Methodology concepts and cases " 2ndedition, Vikas Publishing house pvt ltd.
2. Michael Quinn Patton "Qualitative Research & Evaluation Methods" 3rd edition, Sage Publications
3. Paul D. Leedy,Jeanne Ellis Ormrod "Practical Research: Planning and Design", Prentice Hall

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	1						1	1	1	3	2	
CO2	3	2	2	1						1	1	1	3	2	
CO3	3	2	2	1						1	1	1	3	2	
CO4	3	2	2	1						1	1	1	3	2	
CO5	3	2	2	1						1	1	1	3	2	
CO6	3	2	2	1						1	1	1	3	2	

21PVD01	DEVICE MODELING-I	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- To study the MOS capacitors and to model MOS Transistors
- To understand the various CMOS design parameters and their impact on performance of the device
- To study the device level characteristics of BJT transistors

UNIT I MOS CAPACITORS 9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Non equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics,High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling,Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown

UNIT II MOSFET DEVICES 9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Sub threshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, ShortChannel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High fields

UNIT III CMOS DEVICE DESIGN 9

MOSFET Scaling, Constant-Field Scaling, Generalized Scaling, Non scaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Non uniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length,Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements

UNIT IV CMOS PERFORMANCE FACTORS 9

Basic CMOS Circuit Elements, CMOS Inverters, CMOS NAND and NOR Gates, Inverter and NAND Layouts, Parasitic Elements, Source–Drain Resistance, Parasitic Capacitances, Gate Resistance, Interconnect R and C, Sensitivity of CMOS Delay to Device Parameters, Propagation Delay and Delay Equation, Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness, Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage, Sensitivity of Delay to Parasitic Resistance and Capacitance, Delay of Two-Way NAND and Body Effect, Performance Factors of Advanced CMOS Devices, MOSFETs in RF Circuits, Effect of Transport Parameters on CMOS Performance, Low-Temperature CMOS.

UNIT V BIPOLAR DEVICES 9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base– Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Non ideal Base Current at Low

Currents, Bipolar Device Models for Circuit and Time-Dependent- Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter
Diffusion Capacitance, ChargeControl Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base– Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between BVCEO and BVCBO.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Design MOS capacitors and to model MOS Transistors.

CO2 Design and model MOSFET devices to desired specifications.

CO3 Design and model BJT devices to desired specifications.

C04 Design and model of CMOS device.

C05 Design of Bipolar devices.

C06 Design an application or software for a product.

REFERENCE BOOKS

1. Behzad Razavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2ndEdition
2. J P Collinge, C A Collinge, “Physics of Semiconductor devices” Springer 2002Edition.
3. Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	1	2					1		2	3	2	
CO2	3	2	2	1	2					1		2	3	2	
CO3	3	2	2							1		2	3	2	
CO4	3	2	2							1		2	3	2	
CO5	3	2	2	1	2					1		2	3	2	
CO6	3				2					1		2	3	2	

21PVD02	RF IC DESIGN	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- To study the various impedance matching techniques used in RF circuit design.
- To understand the functional design aspects of LNAs, Mixers, PLLs and VCO.
- To understand frequency synthesis.

UNIT I IMPEDANCE MATCHING IN AMPLIFIERS 9

Definition of ‚Q', series parallel transformations of lossy circuits, impedance matching using , L' PI' and T networks, Integrated inductors, resistors, Capacitors, tunable inductors, transformers

UNIT II AMPLIFIER DESIGN 9

Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs. Principles of RF Power Amplifiers design

UNIT III ACTIVE AND PASSIVE MIXERS 9

Qualitative Description of the Gilbert Mixer - Conversion Gain, and distortion and noise , analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV OSCILLATORS 9

LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer, Basic Fractional-N frequency synthesizer

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Understand the principles of operation of an RF receiver front end

CO2 Design active and passive mixers.

CO3 Design and apply constraints for LNAs, Mixers and Frequency synthesizers

CO4 Design and apply types of oscillators.

CO5 Design and apply PLL and synthesizer.

CO6 Understand and implement the concepts of RF IC design.

REFERENCE BOOKS

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999
4. Jia-sheng Hong, "Microstrip filters for RF/Microwave applications", Wiley, 2001
5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits", Cambridge University Press ,2003

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	2	2	2		2					2				
CO2	3	2	2	2		2					2				
CO3	3	2	2	2		2					2	2	3	2	
CO4	3	2	2	2		2					2	2	3	2	
CO5	3	2				2					2	2	3	2	
CO6	3	2				2					2	2	3	2	

21PVD03	DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- This course deals with CMOS circuit design of various Analog Filter architectures.
- The required signal conditioning techniques in a Mixed signal IC environment are also dealt in this course.
- To study signal conditioning circuits.

UNIT I FILTER TOPOLOGIES 9

The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, the Digital Biquad.

UNIT II INTEGRATOR REALIZATION 9

Lowpass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active RC SNR, gm-C Integrators, Discrete Time Integrators.

UNIT III SWITCHED CAPACITOR FILTER REALIZATION 9

Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth effects, Layout consideration, Noise in SC Filters.

UNIT IV SIGNAL CONDITIONING TECHNIQUES 9

Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for capacitive sensors, Noise and Drift in Resistors, Layout Techniques.

UNIT V SIGNAL CONDITIONING CIRCUITS 9

Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Transimpedance Amplifiers, Charge Amplifiers, Noise in Amplifiers

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Apply the operational and design principles for all the important active analog filter configurations.

CO2 Gain working knowledge of signal conditioning techniques

CO3 Gain the necessary guide lines in a Mixed signal IC environment.

CO4 Apply the techniques in filter realization.

CO5 Design and implementation of Amplifiers.

CO6 Implementation of Analog filters in the applications.

REFERENCE BOOKS

1. Ramson Pallas-Areny, John G. Webster “Sensors and Signal Conditioning” , A wiley Inter science Publication, John Wiley & Sons INC,2001.
2. R.Jacob Baker, ”CMOS Mixed-Signal Circuit Design”, John Wiley & Sons, 2008
3. Schauman, Xiao and Van Valkenburg, “Design of Analog Filters”, Oxford University Press, 2009.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	2	3	2							1	3	3	2	
CO2	3	2	3	2							1	3	3	2	
CO3	3	2	3	2							1	3	3	2	
CO4	3	2	3	2	2	3					1	3	3	2	
CO5	3	2	3	2	2	3					1	3			
CO6	3	2	3	2	2	3					1	3			

21PVD04	NANO SCALE DEVICES	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- To introduce novel MOSFET devices and understand the advantages of multi-gate devices
- To introduce the concepts of nanoscale MOS transistor and their performance characteristics
- To study the various nano scaled MOS transistors

UNIT I INTRODUCTION TO NOVEL MOSFETS 9

MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter subband scattering, multigate technology – mobility – gate stack

UNIT II PHYSICS OF MULTIGATE MOS SYSTEMS 9

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility

UNIT III NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE 9

Silicon nanowire MOSFETs – Evaluvation of I-V characteristics – The I-V characteristics for non-degenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single electron charging – Single electron transistors.

UNIT IV RADIATION EFFECTS 9

Radiation effects in SOI MOSFETs, total ionizing dose effects – single gate SOI – multigate devices, single event effect, scaling effects

UNIT V CIRCUIT DESIGN USING MULTIGATE DEVICES 9

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance - intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Design circuits using nano scaled MOS transistors with the physical insight of their functional characteristics.

CO2 Gain knowledge of 1D and 2D channels.

CO3 Design circuits using multigate devices.

CO4 Analyze of SOI and MOSFET.

CO5 Design of Multigate devices.

CO6 Design and implementation of Nano Scale technology.

REFERENCE BOOKS

1. J P Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2008
2. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006
3. M S Lundstorm, "Fundamentals of Carrier Transport", 2nd Ed., Cambridge University Press, Cambridge UK, 2000

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	1			2						3	1	2	2	
CO2	3	1			2						3	1	2	2	
CO3	3	1	2	1	2						3			2	
CO4	3	1	2	1	2						3	1	2	2	
CO5	3	1	2	1	2						3	1	2	2	
CO6	3	1	2	1	2						3	1			

21PVD05	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

The objective of this course is to provide in-depth knowledge on

- Digital Signal Processor basics
- Third generation DSP Architecture and programming skills
- Advanced DSP architectures and some applications.

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs 9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs –Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II SPECIAL FUNCTIONS 9

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III LINEAR PROGRAMMING 9

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files – Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

UNIT IV ALGEBRAIC EQUATIONS 9

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V ORDINARY DIFFERENTIAL EQUATIONS 9

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Become Digital Signal Processor specialized engineer

CO2 DSP based System Developer

CO3 Gain knowledge of various processors.

CO4 Implementation of ADSP architectures.

CO5 Implementation of TMS320C54X architectures.

CO6 Implementation and design of DSP processor and architectures.

REFERENCE BOOKS

1. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, cengage Learning India Private Limited, Delhi 2012

2. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications" – Tata McGraw – Hill Publishing Company Limited. New Delhi,2003
3. Rulph Chassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A John Wiley & Sons, Inc., Publication,2005
4. User guides Texas Instrumentation, Analog Devices,Motorola.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	3	2		2				1				1	
CO2			3	2		2				1		2	3	1	
CO3	3	2	3	2		2				1		2	3	1	
CO4	3	2	3	2		2				1		2	3	1	
CO5	3	2	3	2		2				1		2	3	1	
CO6	3	2	3	2		2				1				1	

21PVD06	NETWORKS ON CHIP	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

The students should be made to:

- Understand the concept of network - on - chip
- Learn router architecture designs
- Study fault tolerance network - on –chip

UNIT I INTRODUCTION TO NOC 9

Introduction to NoC – OSI layer rules in NoC - Interconnection Networks in Network-on-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support.

UNIT II ARCHITECTURE DESIGN 9

Switching Techniques and Packet Format - Asynchronous FIFO Design -GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design – Adaptive Router Architecture Design.

UNIT III ROUTING ALGORITHM 9

Packet routing-Qos, congestion control and flow control – router design – network link design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing for 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms

UNIT IV TEST AND FAULT TOLERANCE OF NOC 9

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on-Chips.

UNIT V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP 9

Three-Dimensional Networks-on-Chips Architectures. – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation for QoS On-Chip Communication – Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-on-Chip

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Compare different architecture design

CO2 Discuss different routing algorithms

CO3 Explain three dimensional networks - on-chip architectures

CO4 Discuss the concepts of Testing and Fault.

CO5 Design and discuss the concepts of networks -on-chip.

CO6 Study and analyze the networks on chip.

REFERENCE BOOKS

1. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on - Chip " Architectures Holistic Design Exploration", Springer.
2. Fayezgebali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi "Networks-on-Chips theory and practice CRC press.
3. Konstantinos Tatas and Kostas Siozios"Designing 2D and 3D Network-on-Chip Architectures"2013
4. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip"2014
5. SantanuKundu, Santanu Chattopadhyay "Network-on-Chip: The Next Generation of System on-Chip Integration",2014 CRC Press

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO1 0**	**PO1 1**	**PO1 2**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	1	3						2	2	2	1	
CO2	3	2	2	1	3						2	2	2	1	
CO3	3	2	2	1	3						2	2	2	1	
CO4	3	2	2	1	3						2	2	2	1	
CO5	3	2	2	1	3						2	2	2	1	
CO6	3	2	2	1	3						2	2	2	1	

21PVD07	SIGNAL INTEGRITY FOR HIGH SPEED DESIGN	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics
- To study about the clock distribution.

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skineffect, dispersion

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and farend cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current ,Connectors

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Identify sources affecting the speed of digital circuits

CO2 Improve the signal transmission characteristics.

CO3 Gain knowledge about clock distribution and clock oscillators.

CO4 Study the concepts of power used in the system design.

CO5 Identify the clock distribution in the system.

CO6 Gain Knowledge in the Signal transition in the system.

REFERENCE BOOKS

1. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR,2003.
2. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR,2003
3. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall,1993.
4. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience,2000.
5. SPICE, source -http://www-cad.eecs.berkeley.edu/Software/software.html
6. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html SPECCTRAQUEST from Cadence,http://www.specctraquest.com

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	2		1					2	1	3	2	
CO2	3	2	2	2	1	1					2	1	3	2	
CO3	3	2	2	2		1					2	1	3	2	
CO4	3	2	2	2	1	1					2	1	3	2	
CO5	3	2	2	2		1					2	1	3	2	
CO6	3	2	2	2	1	1					2	1	3	2	

21PVD08	DIGITAL CONTROL ENGINEERING	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- Students should acquire a fundamental understanding of digital control systems and design.
- To teach the fundamental concepts of Digital Control systems and mathematical modeling of the system
- To study the concept of time response and frequency response of the discrete time system

UNIT I PRINCIPLES OF CONTROLLERS 9

Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9

Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Acquire working knowledge of discrete system science-related mathematics.

CO2 Design a discrete system, component or process to meet desired needs.

CO3 Identify, formulate and solve discrete control engineering problems.

CO4 Improve the concepts in digital control Algorithms.

CO5 Study the concepts in digital control algorithms.

CO6 Design and Implementation of digital concepts.

REFERENCE BOOKS

1. JohnJ.D'Azzo,"Constantive Houpios, Linear Control System Analysis and Design",McGrawHill,1995.

2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition,1996.
3. M. Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi,1997.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	1	1	2	2				1	1	1	3	2	
CO2	3	2	1	1	2	2				1	1	1	3	2	
CO3	3	2	1	1	2	2				1	1	1	3	2	
CO4	3	2	1	1	2	2				1	1	1	3	2	
CO5	3	2	1	1	2	2				1	1	1	3	2	
CO6	3	2	1	1	2	2				1	1	1	3	2	

21PVD09	EMBEDDED SYSTEM DESIGN	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

The students should be made to:

- Learn design challenges and design methodologies
- Study general and single purpose processor
- Understand bus structures

UNIT I EMBEDDED SYSTEM OVERVIEW 9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer‟s view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analogto-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES 9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS 9

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Explain different protocols

CO2 Discuss state machine and design process models

CO3 Outline embedded software development tools and RTOS

CO4 Study and analyze of state machines.

CO5 Identify the tools in embedded syatem design.

CO6 Study and design of Embedded concepts.

REFERENCE BOOKS

1. Bruce Powel Douglas, “Real time UML, second edition: Developing efficient objects for embedded systems”, 3rd Edition 1999, Pearson Education.
2. Daniel W. Lewis, “Fundamentals of embedded software where C and assembly meet”, Pearson Education,2002
3. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & sons,2002.
4. Steve Heath, “Embedded System Design”, Elsevier, Second Edition,2004.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	2	1	2		1						2	2	1	
CO2	3	2	1	2	1	2								1	
CO3	3	2	1	2										1	
CO4	3	2	1	2	2	2								1	
CO5	3	2	1	2								2	2	1	
CO6	3	2	1	2	3	3						2	2	1	

21PVD10	SOFT COMPUTING AND OPTIMIZATION TECHNIQUES	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- To learn various Soft computing frameworks.
- To familiarizes with the design of various neural networks.
- To understand the concept of fuzzy logic.

UNIT I NEURAL NETWORKS 9

Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks– Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network

UNIT II FUZZY LOGIC 9

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making

UNIT III NEURO-FUZZY MODELING 9

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – NeuroFuzzy Control – Case Studies.

UNIT IV CONVENTIONALOPTIMIZATION TECHNIQUES 9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient, conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization – sequential linear programming, Interior penalty function method, external penalty function method.

UNIT V EVOLUTIONARY OPTIMIZATION TECHNIQUES 9

Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Implement machine learning through Neural networks.

CO2 Develop a Fuzzy expert system.

CO3 Model Neuro Fuzzy system for clustering and classification.

CO4 Identify the optimization techniques.

CO5 Study the concepts of optimization techniques and algorithms.

CO6 Implementation and design of various soft computing frameworks.

REFERENCE BOOKS

1. David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley,2009
2. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Prentice Hall,1995.
3. James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn.,2003.
4. Jyh-Shing Roger Jang, Chuen-Tsai Sun, EijiMizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India,2003.
5. Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall,1998
6. Simon Haykins, Neural Networks: A Comprehensive Foundation,Prentice Hall International Inc,1999.
7. Singiresu S. Rao, Engineering optimization Theory and practice, John Wiley & sons, inc, Fourth Edition,2009
8. Timothy J.Ross, Fuzzy Logic with Engineering Applications, McGraw-Hill,1997.
9. Venkata Rao, Vimal J. Savsani, Mechanical Design Optimization Using Advanced Optimization Techniques, springer2012

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	2		1						3	1	1	
CO2	3	2		2		1						3			
CO3	3	2		2		1						2	3	1	
CO4	3	2		2		1							1	1	
CO5	3	2	2	2		1						2	1	1	
CO6	3	2	2	2		1						3	1	1	

21PVD11	RECONFIGURABLE ARCHITECTURES	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

The students should be made to:

- Understand concept of reconfigurable systems
- Learn programmed FPGAs
- Study flexibility on routability

UNIT I INTRODUCTION **9**

Domain-specific processors, Application specific processors, Reconfigurable Computing Systems –Evolution of reconfigurable systems – Characteristics of RCS advantages and issues. Fundamental concepts & Design steps –classification of reconfigurable architecture-fine, coarse grain & hybrid architectures – Examples

UNIT II FPGA TECHNOLOGIES&ARCHITECTURE **9**

Technology trends- Programming technology- SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks – CLB Vs LAB Vs Slices- Fast carry chains- Embedded RAMs- FPGA Vs ASIC design styles.

UNIT III ROUTING FOR FPGA **9**

General Strategy for routing in FPGAs- routing for row-based FPGAs – segmented channel routing, definitions- Algorithm for I segment and K segment routing – Routing for symmetrical FPGAs, flexibility of FPGA Routing Architectures: FPGA architectural flexibility on Routability Effect of switch block flexibility on routability - Tradeoffs in flexibility of S and C blocks

UNIT IV HIGH LEVEL DESIGN **9**

FPGA Design style: Technology independent optimization- technology mapping- Placement. Highlevel synthesis of reconfigurable hardware, high- level languages, Design tools: Simulation (cycle based, event driven based) – Synthesis (logic/HDL vs physically aware) – timing analysis (static vs dynamic)- verification physical design tools.

UNIT V APPLICATION DEVELOPMENT WITH FPGAS 9

Case Studies of FPGA Applications–System on a Programmable Chip (SoPC) Designs.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Compare FPGA routing architectures

CO2 Discuss FPGA applications

CO3 Explain high level synthesis

CO4 Understand the concepts of physical verification tools

CO5 Knowledge about the Synthesis tools

CO6 Study about the design and verification tools in VLSI design

REFERENCE BOOKS

1. Christophe Bobda, "Introduction to Reconfigurable Computing –Architectures, Algorithms and Applications", Springer,2010.
2. Clive "Max" Maxfield, "The Design Warrior"s Guide to FPGAs: Devices, Tools And Flows", Newnes, Elsevier,2006
3. Jorgen Staunstrup, Wayne Wlf, "Hardware/Software Co- Design: Priciples and practice", Kluwer Academic Pub,1997.
4. MayaB.GokhaleandPaulS.Graham,"ReconfigurableComputing:AcceleratingComputation in Field-Programmable Gate Arrays", Springer,2005.
5. Russell tessier and Wayne Burleson "Reconfigurable Computing for Digital Signal Processing: A Survey" Journal of VLSI Signal processing 28,p7-27,2001.
6. Stephen M. Trimberger, "field – programmable Gate Array Technology"Springer,2007.
7. Stephen D. broen, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic," Field programmable Gate Arrays", Kluwer Academic Pubnlishers,1992.
8. Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing –The Theory and Practice of FPGA-Based Computation", Elsevier / Morgan Kaufmann,2008.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	1	2							3	3	1	2	
CO2	3	2	1	2							3	3	1	2	
CO3	3	2	1	2							3	3	1	2	
CO4	3	2	1	2							3	3	1	2	
CO5	3	2	1	2							3	3	1	2	
CO6	3	2	1	2							3	3	1	2	

21PVD12	ADVANCED MICROPROCESSOR AND ARCHITECTURES	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- To study 80386 and Pentium processor
- To understand CISC and RISC Architectures
- To Learn ARM processor

UNIT I 80386 AND PENTIUM PROCESSOR 9

80386 PROCESSOR: Basic programming model – Memory organization – Data types – Instruction set - Addressing mode – Address translation – Interrupts –PENTIUM PROCESSOR : Introduction to Pentium processor architecture – Special Pentium Registers – Pentium Memory Management – Introduction to Pentium pro processor – Pentium Pro Special Features.

UNIT II CISC AND RISC ARCHITECTURE 9

Introduction to RISC architectures: RISC Versus CISC – RISC Case studies: MIPS R4000 – SPARC – Intel i860 - IBMRS/6000

UNIT III ARM PROCESSOR 9

ARM Programmer's Model– Registers–Processor Modes– State of the processor– Condition Flags – ARM Pipelines – Exception Vector Table – ARM Processor Families – Typical 3 stage pipelined ARM organization–Introduction to ARM Memory Management Unit.

UNIT IV ARM ADDRESSING MODES AND INSTRUCTION SET 9

ARM Addressing Modes – ARM Instruction Set Overview – Thumb Instruction Set Overview – LPC210X ARM Processor Features.

UNIT V PIC MICROCONTROLLER AND MOTOROLA 68HC11 MICROCONTROLLER 9

Instruction set, addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART. MOTOROLA: CPU Architecture – Instruction set – interrupts- TimersI 2C Interfacing –UART- A/D Converter – PWM

COURSE OUTCOMES

At the end of the course, a student will be able to

CO1 Discuss ARM addressing modes

CO2 Outline ARM instruction set

CO3 Explain PIC microcontroller and motorola 68HC11microcontroller

CO4 Study of ARM and its addressing modes.

CO5 Study of PIC microcontroller.

CO6 Design and study of advanced processors and architectures.

REFERENCE BOOKS

1. Andrew Sloss, "ARM System Developer"s Guide", Morgan Kaufmann Publishers,2005
2. Barry B Brey, "The Intel Microprocessor, Pentium and Pentium Pro Processor, Architecture Programming and Interfacing", Prentice Hall of India,2002
3. Daniel Tabak, "Advanced Microprocessors", McGraw Hill Inc.,1995
4. David E Simon "An Embedded Software Primer", Pearson Education,2007
5. Gene .H.Miller ." Micro Computer Engineering ," Pearson Education ,2003.
6. Intel, "Microprocessors, Vol-I & Vol-II", Intel Corporation, USA,1992.
7. John .B.Peatman , " Design with PIC Microcontroller , Prentice hall,1997
8. Mohammed Rafiquzzaman, "Microprocessors and Microcomputer Based System Design", Universal Book Stall, New Delhi, 1990.
9. Steve Furber, "ARM System-on-Chip Architecture", Pearson Education, 2005 "ARM7 TDMI Technical Reference Manual", ARM Ltd., UK, 20046.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	2	1	2	1	1				2			3	2	
CO2	3	3	3	2	1	2				2			3	2	
CO3	3	2	1	2	1	1				2			3	2	
CO4	3	2	1	2	1	1				2			3	2	
CO5	3	2	2	2	1	3				2			3	2	
CO6	3	2	1	2	1	1				2			3	2	

21PVD13	SELECTED TOPICS IN ASIC DESIGN	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- The course focuses on the semi-custom IC Design and introduces the principles of design logic cells, I/O cells and interconnects architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti-fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECUTRE 9

Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENTAND ROUTING 9

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

UNIT V HIGH PERFORMANCE ALGORITHMS FOR ASICS/ SOCS, SOC CASES STUDIES 9

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case Studies: Digital camera, SDRAM, High speed data standards.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Understand the knowledge in the circuit design aspects at the next transistor and block Level abstractions of FPGA and ASIC design.

CO2 Know the concept of CAD for VLSI

CO3 Understand sufficient theoretical knowledge for carrying out FPGA and ASIC designs.

CO4 Study of logical synthesis.

CO5 Identify and implement ASIC Soc algorithms.

CO6 Analyze of routing and placement.

REFERENCE BOOKS

1. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications,1996
2. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall,1994.
3. M.J.S.Smith, " Application - Specific Integrated Circuits",Pearson,2003
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill,1994.
5. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, "FPGA-based Implementation of Signal Processing Systems", Wiley,2008
6. Steve Kilts, "Advanced FPGA Design," Wiley Inter-Science.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	3	2	1	2						2	2	1	
CO2	3	2				3						2	3	1	
CO3	3	2	3	2	1	2						2	2	1	
CO4	3	2	3	2		2								1	
CO5	3	2	3	2		2						2	3	1	
CO6	3	2	1	2	1	2						2	2	2	

		L	T	P	C
21PVD14	**DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS**	**2**	**0**	**2**	**3**

COURSE OBJECTIVES

- To discuss the algorithmic complexity parameters and the basic algorithmic design techniques.
- To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems.
- To study various algorithms.

UNIT I INTRODUCTION 9

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES 9

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING 9

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

UNIT IV GRAPH ALGORITHMS 9

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm

UNIT V SELECTED TOPICS 9

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Apply the suitable algorithm according to the given optimization problem.

CO2 Modify the algorithms to refine the complexity parameters.

CO3 Gain knowledge on graph algorithms.

CO4 Analyze the graph algorithms.

CO5 Discuss the concepts in NP algorithms.

CO6 Apply and analyze the complexity parameters and NP agorithms.

REFERENCE BOOKS

1. D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley,1989
2. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms",Galgotia Publications,1988.
3. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis",Addison

Wesley,1988.
4. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill,1994.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	2	1	2		2					1	2	1	2	
CO2	3	2	2	3	3	2					1	2	1	2	
CO3	3	2			2	2					1	2	1	2	
CO4	3	2		1	2	2					1	2	1	2	
CO5	3	2				2					1	2	1	2	
CO6	3	2	1	2	1	2					1	2	1	2	

21PVD15	DEVICE MODELING–II	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

- To understand device physics and device modeling aspects
- To study simulators to characterize the device models
- To study multistep methods.

UNIT I MOSFET DEVICE PHYSICS 9

MOSFET Basic operation, Level 1, Level 2, Level 3 models, Noise sources in MOSFET, Flicker noise modeling, Thermal noise modelling, Influence of process variation, modeling of device mismatch for Analog/RF Applications

UNIT II DEVICE MODELLING 9

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability

UNIT III MULTISTEP METHODS 9

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V SIMULATION OF DEVICES 9

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Design and model MOSFET devices, taking into consideration process dependent parameters

CO2 Utilize device level simulators

CO3 Gain knowledge on device physics and device modeling aspects

CO4 Analyze the concepts for device simulations.

CO5 Discuss the concepts of computational characteristics.

CO6 Analyze the concepts of device models.

REFERENCE BOOKS

1. Arora, N., “MOSFET Models for VLSI Circuit Simulation”, Springer-Verlag,1993
2. Chua, L.O. and Lin, P.M., “Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques”, Prentice-Hall.,1975
3. Fjeldly, T., Yetterdal, T. and Shur, M., “Introduction to Device Modeling and Circuit Simulation”,Wiley-Interscience.,1997
4. Grasser, T., “Advanced Device Modeling and Simulation”, World Scientific Publishing Company.,2003

5. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag.,1984
6. Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & SonsLtd.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	1	2	2					2	2	1	2	2	
CO2	3	2	2	3						2	2	3		2	
CO3	3	2	3		1					2	3		1	2	
CO4	3	2		3						2		3		2	
CO5	3	2			2					2			2	2	
CO6	3	2	1	2	2					2	2	1	2	2	

21PVD16	DIGITAL IMAGE PROCESSING	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

The students should be made to:

- Understand fundamentals of digital images
- Learn different image transforms
- Study concept of segmentation

UNIT I DIGITAL IMAGE FUNDAMENTALS 9

A simple image model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different types of digital images. Basic concepts of digital distances, distance transform, medial axis transform, component labeling, thinning, morphological processing, extension to gray scale morphology.

UNIT II IMAGE TRANSFORMS 9

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III SEGMENTATION OF GRAY LEVEL IMAGES 9

Histogram of gray level images, multilevel thresholding, Optimal thresholding using Bayesian classification, Watershed and Dam Construction algorithms for segmenting gray level image. Detection of edges and lines: First order and second order edge operators, multi-scale edge detection, Canny's edge detection algorithm, Hough transform for detecting lines and curves, edge linking.

UNIT IV IMAGE ENHANCEMENT AND COLOR IMAGE PROCESSING 9

Point processing, Spatial Filtering, Frequency domain filtering, multi-spectral image enhancement,image restoration. Color Representation, Laws of color matching, chromaticity diagram, color enhancement, color image segmentation, color edge detection, color demosaicing.

UNIT V IMAGE COMPRESSION 9

Lossy and lossless compression schemes, prediction based compression schemes, vector quantization, sub-band encoding schemes, JPEG compression standard, Fractal compression scheme, Wavelet compression scheme.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Discuss image enhancement techniques

CO2 Explain color image processing

CO3 Compare image compression schemes

CO4 Study the concepts of image enhancement.

CO5 Analyze the concepts of image compression.

CO6 Identify the concepts of digital image processing.

REFERENCE BOOKS

1. A.K. Jain, "Fundamentals of Digital Image Processing", Prentice-Hall, AddisonWesley,1989.
2. Bovik (ed.), "Handbook of Image and Video Processing", Academic Press,2000.
3. B. Jähne, "Practical Handbook on Image Processing for Scientific Applications", CRC Press,1997.
4. Bernd Jähne, Digital Image Processing, Springer-Verlag Berlin Heidelberg 2005.
5. Gonzalez and Woods, Digital Image Processing,Prentice-Hall.
6. J. C. Russ. The Image Processing Handbook. CRC, Boca Raton, FL, 4th edn.,2002.
7. J. S. Lim, "Two-dimensional Signal and Image Processing" Prentice-Hall,1990.
8. M. Petrou, P. Bosdogianni, "Image Processing, The Fundamentals", Wiley,1999.
9. Rudra Pratap, Getting Started With MATLAB 7. Oxford University Press,2006
10. Stephane Marchand-Maillet, Yazid M. Sharaiha, Binary Digital Image Processing, A Discrete Approach, Academic Press, 2000
11. W. K. Pratt. Digital image processing, PIKS Inside. Wiley, New York, 3rd, edn.,2001.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO1 0**	**PO1 1**	**PO1 2**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	3	2	2	1						1	3	1	2	
CO2	3	3	2		1						1	3	1	2	
CO3	3	3		2	1						1	3	1	2	
CO4	3	3	1		1						1	2	3	2	
CO5	3	3			1						1	3	1	2	
CO6	3	3	2	2	1						1	3	2	2	

21PVD17	MEMS AND NEMS	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- To introduce the concepts of micro electromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and microactuators.

UNIT I OVERVIEW **9**

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS:Silicon, silicon compounds, polymers, metals.

UNIT II MEMS FABRICATION TECHNOLOGIES **9**

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micro machining,High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

UNIT III MICROSENSORS **9**

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV MICRO ACTUATORS **9**

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS **9**

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Discuss microsensors.

CO2 Explain microactuators.

CO3 Outline nanosystems and Quantum mechanics.

CO4 Discuss the concepts of actuators.

CO5 Study of nano and quantum mechanics.

CO6 Design and study the concepts of micro sensors and fabrication process.

REFERENCE BOOKS

1. Chang Liu, “Foundations of MEMS”, Pearson education India limited,2006.
2. Marc Madou, “Fundamentals of Microfabrication”, CRC press1997.
3. Stephen D. Senturia,” Micro system Design”, Kluwer AcademicPublishers,2001
4. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures” CRC Press,2002.
5. Tai Ran Hsu ,”MEMS and Microsystems Design and Manufacture” ,Tata Mcraw Hill,2002.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO1 0**	**PO1 1**	**PO1 2**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	1	2		1				1		3	1	2	
CO2	3	2	1	2		1				1		3	1	2	
CO3	3	2	1	2		1				1		3	1	2	
CO4	3	2	1	2		1				1		3	1	2	
CO5	3	2	1	2		1				1		3	1	2	
CO6	3	2	1	2		1				1		3	1	2	

21PVD18	SCRIPTING LANGUAGES FOR VLSI	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

The students should be made to:

- Study scripting languages
- Understand security issues
- Learn concept of TCL phenomena

UNIT I INTRODUCTION TO SCRIPTING AND PERL 9

Characteristics of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions,Subroutines, Scripts with arguments.

UNIT II ADVANCED PERL 9

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects,Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT III TCL 9

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT IV ADVANCED TCL 9

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running un trusted code, The C interface.

UNIT V TK AND JAVASCRIPT 9

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Explain advanced TCL

CO2 Discuss TK and Java script

CO3 To gain knowledge on security issues

CO4 Understand the concepts of marketing applications.

CO5 Study the fundamental concepts of TK.

CO6 To understand the Scripting languages used in VLSI systems.

REFERENCE BOOKS

1. Brent Welch,"Practical Programming in Tcl and Tk",Fourth Edition,2003.
2. David Barron, "The World of Scripting Languages", Wiley Publications,2000.
3. Guido van Rossum, and Fred L. Drake ", Python Tutorial, Jr., editor, Release 2.6.4 Randal L.Schwartz,"Learning PERL", Sixth Edition,O‟Reilly

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2	PSO3
CO1	3	2	2	2							1	1	3	2	
CO2	3	3	2	1								1	3	2	
CO3	3	2	2	2								1	3	2	
CO4	3	1	2	3							2	1	3	2	
CO5	3	2	2	2							3	1	3	2	
CO6	3	2	2	2								1	3	2	

21PVD19	HARDWARE –SOFTWARE CO-DESIGN	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- To acquire the knowledge about system specification and modelling.
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches,Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE /SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE / SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, CoSynthesis Algorithm for Distributed System- Case Studies with any one application

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping ,Target Architecture, Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification ,Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Assess prototyping and emulation techniques

CO2 Compare hardware / software co-synthesis.

CO3 Formulate the design specification and validate its functionality by simulation

CO4 Explain the protyping and its techniques.

CO5 Study of system level synthesis and its verification languages.

CO6 Discuss the protyping architectures and its applications.

REFERENCE BOOKS

1. Giovanni De Micheli , Rolf Ernst Morgon," Reading in Hardware/Software Co-Design" KaufmannPublishers,2001.
2. Jorgen Staunstrup, Wayne Wolf ,"Hardware/Software Co-Design: Principles and Practice" , Kluwer AcademicPub,1997.
3. Ralf Niemann , "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub,1998.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	1	1		2						1	2	1	
CO2	3	2	1	1		2						1	2	2	
CO3	3	3	2	1								1	1		
CO4	3		1	1		1						2		3	
CO5	3	2	1	1		2						1	2	2	
CO6	3	2	1	1		2						1	2	2	

21PVD20	SELECTED TOPICS IN IC DESIGN	L	T	P	C
		2	0	2	3

COURSE OBJECTIVES

- This course deals with the supply circuit modules which are crucial modules in an IC design.
- Clock generation circuits play a major role in High Speed Broad Band Communication circuits, High Speed I/O‟s, Memory modules and Data Conversion Circuits.
- This course focuses on the design aspect of Clock Generation circuits and their design constraints.

UNIT I VOLTAGE AND CURRENT REFERENCES 9

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing.

UNIT II LOW DROPOUT REGULATORS 9

Analog Building Blocks, Negative Feedback, AC Design, Noise and Noise Reduction Techniques, Stability, LDO Efficiency, LDO Current Source, LDO Current Source Using Opamp..

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV PHASE LOCKLOOPS 9

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance.

UNIT V CLOCK AND DATA RECOVERY 9

CDR Architectures, Tias and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Know how to a designer to construct Supply reference circuits and Clock Generation Circuits for given design specifications and aids the designer

CO2 Understand High Speed I/O‟s,Memory modules and Data Conversion Circuits

CO3 Understand the design specifications related to Supply and Clock Generation Circuits.

CO4 Discuss the concepts of PLL and its topology.

CO5 Study and implement the CDR architecture.

CO6 Understand the concept of clock generation and their design constraints.

REFERENCE BOOKS

1. BehzadRazavi, " Design of Integrated circuits for Optical Communications", McGraw Hill, 2003.
2. Floyd M. Gardner ,"PhaseLocK Techniques" John wiley& Sons, Inc 2005.
3. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgapcircuits",Johnwiley& Sons, Inc 2002.
4. High Speed Clock and Data Recovery, High-performance Amplifiers Power Management" springer, 2008.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	2		1						1	3	2	
CO2	3	2	2	3		1						1		2	
CO3	2	3								1	1	1		2	
CO4	1		1	1		2				1	1	1	3	2	
CO5		1		2		1				1		2		2	
CO6	3	2	2	2		1				1			1	2	

21PVD21	LOW POWER VLSI DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.

UNIT I POWER DISSIPATION IN CMOS 9

Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption –Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques For Leakage Power Reduction - Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION 9

Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform – software design for low power.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Know the basics and advanced techniques in low power design which is a hot topic in today‟s market where the power plays major role.

CO2 Understand reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

CO3 Design low power CMOS circuits.

CO4 Study the concepts of power estimation techniques.

CO5 Discuss the concepts of design of low power system.

CO6 Analyze the techniques to reduce the power dissipation.

REFERENCE BOOKS

1. AbdelatifBelaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
3. DimitriosSoudris, C.Pignet, Costas Goutis,"Designing CMOS Circuits for Low Power"Kluwer,2002.
4. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
5. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons,inc.2001.
6. .J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
7. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.
8. Kiat-send Yeo, Kaushik Roy "Low-Voltage, Low-power VLSI Subsystem", Tata McGrawHill, 2009.

Total:45 Hours

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	2		2					2	1	2	2	
CO2	3	2	2	2		2					2	1	2	2	
CO3	3	2	2	2		2					2	1	2	2	
CO4	3	2	2	2		2					2	1	2	2	
CO5	3	2	2	2		2					2	1	2	2	
CO6	3	2	2	2		2					2	1	2	2	

21AC101 ENGLISH FOR RESEARCH PAPER WRITING L T P C
2 0 0 0

Course objectives:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the goodquality of paper at very first-time submission

Unit I	Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness	5
Unit II	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction	6
Unit III	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	4
Unit IV	Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,	6
Unit V	Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	5
Unit VI	Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission	4

COURSE OUTCOMES

At the end of the course students should be able to

CO1	Know the basic concepts on planning and preparation of paper writing.
CO2	Able to find the research area
CO3	Analysis of various papers in their domain
CO4	Had an idea and clarity to write the paper
CO5	Develop the skills in writing the paper
CO6	Able to write the paper on their own

Text Book

1 Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht HeidelbergLondon, 2011

Reference Books

1 Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)

2 Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press

3 Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													CO/PSO Mapping		
CO s	PROGRAMME OUTCOMES (POs)												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO1	PSO 2	PSO3
CO1	3	2	2	2						2	2	2	3	2	
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CO4	3	2	2	2						2	2	2	3	2	
CO5	3	2	2	2						2	2	2	3	2	
CO6	3	2	2	2						2	2	2	3	2	

21AC201	DISASTER MANAGEMENT	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES

- To provide students an exposure to disasters, their significance and types.
- To ensure that students begin to understand the relationship between vulnerability, disasters, disaster prevention and risk reduction.
- To enhance awareness of institutional processes in the country and
- To develop rudimentary ability to respond to their surroundings with potential disaster response in areas where they live, with due sensitivity.
- To gain a preliminary understanding of approaches of Disaster Risk Reduction (DRR).

UNIT I INTRODUCTION TO DISASTERS 5

Definition: Disaster, Hazard, Vulnerability, Resilience, Risks – Disasters: Types of disasters- Earthquake, Landslide, Flood, Drought, Fire etc – Classification, Causes, Impacts including social, economic, political, environmental and health - Global trends in disasters: urbandisasters complex emergencies, Climate change- Dos and Don'ts during various types of Disasters.

UNIT II APPROACHES TO DISASTER RISK REDUCTION (DRR) 6

Disaster cycle – Phases, prevention, mitigation and preparedness community based DRR, Structural- nonstructural measures, Roles and responsibilities of- Government & NGO's- Institutional Processes and Framework at State and Central Level- State Disaster Management Authority (SDMA) – Early Warning System – Advisories from Appropriate Agencies.

UNIT III INTER-RELATIONSHIP BETWEEN DISASTERS AND DEVELOPMENT 6

Factors affecting Vulnerabilities, impact of Development projects such as dams, embankments, changes in Land-use etc. - Climate Change Adaptation- IPCC and Scenarios in the context of India – Relevance of indigenous knowledge, appropriate technology and local resources.

UNIT IV DISASTER RISK MANAGEMENT IN INDIA 7

Hazard and Vulnerability profile of India, Components of Disaster Relief: Water, Food, Sanitation, Shelter, Health, Waste Management, Disaster Management Act and Policy – Role of GIS and Information Technology Components in Preparedness, Risk Assessment, Response and Recovery Phases of Disaster – Disaster Damage Assessment.

UNIT V DISASTER MANAGEMENT: APPLICATIONS AND CASE STUDIES AND FIELD WORKS 6

atural disasters- Case Studies, Earthquake, Landslide, Drought, Floods: Fluvial and Pluvial Flooding - Man Made disasters: Case Studies, Space Based Inputs for Disaster Mitigation and Management and field works for disaster management.

COURSE OUTCOMES

At the end of the course students should be able to

CO1 To provide students an exposure to disasters

CO2 Analysis of various disaster risk reduction

CO3 Able to find the inter-relationship between disasters and development

CO4 Able to have knowledge about the acts in disaster management

CO5 Study about the natural disasters

CO6 Have a knowledge about the natural disasters and field works in management

REFERNCE BOOKS

1 Singhal J.P. "Disaster Management", Laxmi Publications, 2010.

2 Tushar Bhattacharya, "Disaster Science and Management", McGraw Hill India Educatio Pvt. Ltd., 2012.

3 Gupta Anil K, Sreeja S. Nair. Environmental Knowledge for Disaster Risk Management, NIDM, New Delhi, 2011.

4 Kapur Anu Vulnerable India: A Geographical Study of Disasters, IIAS and Sage Publishers, New Delhi, 2010.

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
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CO3	3	3	2	2	1					1	1	1	3	2	
CO4	3	3	2	2	1					1	1	1	3	2	
CO5	3	3	2	2	1					1	1	1	3	2	
CO6	3	3	2	2	1					1	1	1	3	2	

21AC301 **STRESS MANAGEMENT BY YOGA** **L T P C**
2 0 0 0

Course objectives:

- To enable the student to have good health
- To practice mental hygiene
- To possess emotional stability
- To Integrate moral values
- To attain higher level of consciousness

Unit I	Shatha karma - Kapalbhati (11-30 strokes)Asanas - Trikonasana,Ardha-Kati Chakrasana,Tadasana,Vrikshasana,Padmasana Simhasana, Paschimottanasana, Uttanpadasana,Salabhasana, Shavasana Pranayama – Bhastrika-Concentration – On own breath (2 min) ohm chanting and shanti path	6
Unit II	Shatha karma – Introduction of trataka and practice of concentric on nose– tip. Asanas – Garudasana, EK – Pad Pranamasana kati chakrasana, Urdhava Hastottanasana, Natrajasana , Parvatasana, Kukkutasana, Pawanmuktasana, Bhujangasana, Shavasana Pranayama – Bhramari-Concentration – On own breath (3 min) ohm chanting and shanti path	6
Unit III	Shatha karma – Introduction of Nauli Asanas – Pada Hastasana, Urdhv Pranamasana, Konasana, Vajrasana, Supta Vajrasana, Shashankasana, Gomukhasana, Janusirasana, Naukasana, Halasana, Chakrasana, Shavasana, Surya Namaskar Pranayama – Anuloma-Viloma(Nadishodhan) Concentration – On own breath (So-ham) Ohm Chanting and shanti path.	6
Unit IV	Shatha karma – Jala Neti (if facility Available) Asanas – Trikonasana ,Tadasana, Natrajasana, Kato Chakarasana, Baddhapadmasana, Ushtrasana, Paschimottanasana, Bakasana, Kurmasana, Ardha Marsyendrasana, Makrasana, Dhanurasana, Shavasana, Surya Namaskar Pranayama – Ujjayi and Suryabhedan Concentration – In between eyebrows,Ohm Chanting and shanti path.	6
Unit V	Shatha karma – Trataka Asanas – Trikonasana, Vrikshasana, Parivrat Trikonasana, Padmasana, Yogmudra, Matsyasana, Mandukasana, Vristitapada Bhoonamanasana, Pawanmuktasana, Vipritkarni, Shavasana, Yoganidra Pranayama – Bhramari, Sheetkari Concentration – on 'Dot' or 'Ohm', Ohm Chanting and shanti path.	6

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Able to have knowledge about good health

CO2 Stduents able to practice mental hygiene

CO3 Develop and possess emotional stability

CO4 Study about moral values

CO5 Understand the concepts of level of consciousness

CO6 Have a good health and regular yoga practice

Text Book

1 Yogic Asanas for Group Tarining-Part-I" : Janardan Swami Yogabhyasi Mandal, Nagpur

Reference Books

1 Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata.

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
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CO3	3	2	1	2	2	1						2	3	2	
CO4	3	2	1	2	2	1						2	3	2	
CO5	3	2	1	2	2	1						2	3	2	
CO6	3	2	1	2	2	1						2	3	2	

21AC401	VALUE EDUCATION	L T P C 2 0 0 0

Course objectives:

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Unit I	Values and self-development, Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non, moral valuation. Standards and principles, Value judgements	7
Unit II	Importance of cultivation of values, Sense of duty. Devotion, Self-reliance. Confidence, Concentration, Truthfulness, Cleanliness, Honesty, Humanity. Power offaith, National Unity, Patriotism.Love for nature, Discipline	7
Unit III	Personality and Behavior Development, Soul and Scientific, attitude, positive thinking, Integrity and discipline, Punctuality, Love and Kindness, avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship, Happiness Vs suffering, love for truth, Aware of self- destructive habits, Association and Cooperation, doing best for saving nature	9
Unit IV	Character and Competence, Holy books vs Blind faith, Self-management and Goodhealth, Science of reincarnation, Equality, Nonviolence, Humility, Role of Women, All religions and same message, Mind your Mind, Self-control, Honesty, Studying effectively	7

COURSE OUTCOMES

At the end of the course students should be able to

CO1 Understand the concept value of education and self- development

CO2 Provide Studemts about Imbibe good values

CO3 Able to have some idea about the importance of character

CO4 Understand the concept personality and behaviour development

CO5 Study about the humanity

CO6 Have a knowledge about the humanity and moral valuation

Text Book

1 Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

Reference Book

1 John Haggai “Lead On” & “How to win over worry” – World Book Publisher – 1986

2 Prasantham J.P. “Therapeutic Counselling” – Asian Trading Corporation – 1994

3 Fr. Joe Curie S.J. “Barefoot Counsellor” – aTc Publication – 1998

4 Atkinson D.J. & Field D.H. “New Dictionary of Christian Ethics and Pastoral Theology” – Intervarsity Press, USA – 1995

5 David Clyde Jones “Biblical Christian Ethics” – Baker Books – 1994

CO/PO MAPPING (S/M/W indicates strength of correlation) 3-Strong, 2-Moderate, 1-Fair													**CO/PSO Mapping**		
CO s	**PROGRAMME OUTCOMES (POs)**												**PSOs**		
	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO1 0**	**PO1 1**	**PO1 2**	**PSO1**	**PSO 2**	**PSO3**
CO1	3	2	2	1	1	2						1	3	2	
CO2	3	2	2	1	1	2						1	3	2	
CO3	3	2	2	1	1	2						1	3	2	
CO4	3	2	2	1	1	2						1	3	2	
CO5	3	2	2	1	1	2						1	3	2	
CO6	3	2	2	1	1	2						1	3	2	